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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
**H04L 7/02, 25/497, 25/03**

**A1**

(11) International Publication Number: **WO 98/09400**

(43) International Publication Date: 5 March 1998 (05.03.98)

(21) International Application Number: PCT/IB96/00873

(22) International Filing Date: 30 August 1996 (30.08.96)

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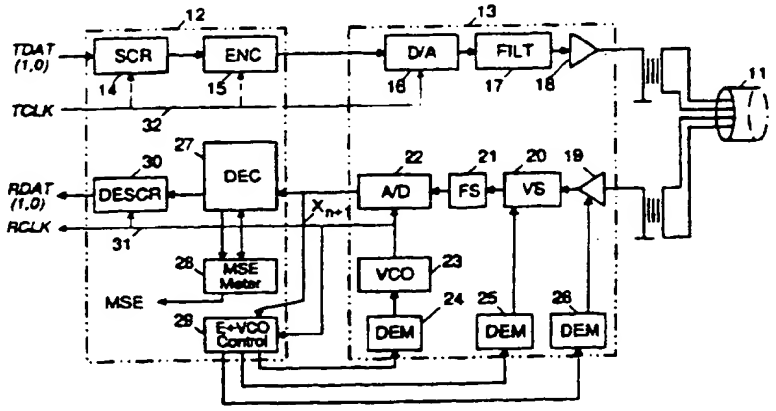
(81) Designated States: JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

**Published**
*With international search report.*

(54) Title: RECEIVING AND EQUALIZING SIGNALS FOR HIGH-SPEED DATA TRANSMISSION




(57) Abstract

Methods and apparatus are disclosed for receiving and/or equalizing data signals transmitted over metallic lines or other means with similar transfer characteristics in communication systems employing multi-level partial-response or full-response signaling. They comprise a novel timing recovery scheme in conjunction with mixed analog/digital or fully digital decision-feedback equalization; this novel scheme avoids false lock situations that can be experienced during initial timing acquisition. Also addressed is the problem of initial convergence of an adaptive decision-feedback equalizer (DFE) in self-training mode. For partial-response systems, the problem is solved by implementing the linear forward filter of the DFE as a two-parameter variable analog filter, for which convergence can be achieved prior to timing recovery. Linear forward equalization by a variable analog filter also leads to the advantage of low power consumption. After initial convergence at the analog filter, decisions obtained at the analog channel output are sufficiently reliable so that timing recovery can be achieved. Then, convergence at the feedback filter of the DFE embedded in an adaptive Viterbi decoder takes place. For full-response systems, fully digital adaptive DFE is used. Timing recovery is accomplished prior to convergence at the linear forward equalizer. Self-training equalization is achieved by a specific method that allows reliable convergence of the coefficients of the DFE to the optimum values.

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DESCRIPTION

# Receiving and Equalizing Signals for High-Speed Data Transmission

## FIELD OF THE INVENTION

This invention relates to transceivers for high-speed, i.e. several Mbit-per-second, data transmission over unshielded twisted-pair cables or other transmission means with similar transfer characteristics. It specifically provides a solution for a low-power transceiver in such systems. One implementation employs quaternary partial-response class-IV (PRIV) signaling in combination with new concepts for mixed adaptive analog and digital equalization, clock recovery, and Viterbi decoding. Another implementation is for full-response systems.

## BACKGROUND AND PRIOR ART

Unshielded twisted-pair (UTP) cables are a preferred transmission medium for many applications that require transmission of data at the speed of several Mbit/sec, in particular for local area networks (LANs). Data transmission systems with UTP cables are also employed to provide high speed connectivity to subscribers over the copper access network, e.g. by high speed digital subscriber lines (HDSLs) or asymmetric digital subscriber lines (ADSLs). Other applications can be found in networks deployed to collect measurement data, e.g. for seismic data acquisition.

In a digital transmission system, data can be recovered from the sequence of samples $x_n$ taken at the output of the overall channel at instants $t = nT+\tau$, where $T$ is the modulation interval, and $\tau$ is a constant sampling phase.

The sample $x_n$ can be expressed in general as the weighted sum

$$x_n = \sum_{i=0}^{N-1} h_i a_{n-i} + w_n ,$$

where $a_n \in A$ is the $n$-th input symbol taken from the symbol set $A$, $h_i$, $i$ = 0, ..., N -1 representing the sampled overall system response and $w_n$ denoting additive noise. In a binary transmission system, the input symbols are taken from the set $A$ = { -1, +1}. Higher spectral efficiency than in binary transmission is obtained by M-ary multi-level transmission, where the symbol set is

$A$ = { -(M-1), ..., -1, +1, ... (M-1)} with M > 2, M even,

$A$ = { -(M-1), ..., -2, 0, +2, ... (M-1)} with M > 2, M odd.

Introducing the $D$-transform notation, the sampled overall response can be expressed by the system polynomial

$$h(D) = \sum_{i=0}^{N-1} h_i D^i ,$$

wherein $D$ denotes the unit-delay operator.

A full-response system is characterized by the absence of intersymbol interference, i.e. $h(D) = 1$. In partial-response systems, intersymbol interference is introduced in a controlled fashion to shape the overall channel response. For example, partial-response class-IV (PRIV), defined by the system polynomial $1-D^2$, is well-suited for DC-free and band-limited transmission over metallic cables because the overall frequency response presents spectral nulls at f = 0 Hz and |f| = $1/2T$ Hz, where $T$ denotes the modulation interval.

Overall signal shaping to full or partial response is obtained by proper design of the filters in the analog and the digital sections at the transmit and receive ends of the transmission link. Signal shaping functions at the receiver usually include variable gain amplification and fixed and adaptive equalization. Signal samples are obtained by analog-to-digital (A/D) conversion of the signal at the analog front-end output at sampling instants that are determined by a timing recovery circuit. In full-response systems, a sampling rate larger than $1/T$ samples/s may be required to avoid

aliasing. In this case, a sequence of signals at a rate of $1/T$ samples/s is obtained at the output of a digital filter that performs the functions of equalization and decimation.

Signal distortion introduced by homogeneous metallic transmission lines is mainly caused by the skin effect. In a receiver for a cable transmission system, signal distortion is usually compensated for by adaptive equalization. Adaptive equalization can be performed either in the analog domain by variable analog filters or in the digital domain, e.g. by adaptive linear transversal filters. A well-known technique for adaptive analog equalization is the automatic line build-out (ALBO) technique. An ALBO equalizer can be described as a combination of a variable-length cable simulator and an appropriate fixed receive filter. Since, for transmission over metallic cables, signal distortion depends essentially on one quantity, i.e. the product of a cable parameter times the cable length, a single control parameter is traditionally adjusted such that a given output signal level is obtained. The combined lengths of the cable and the simulated cable add then up to a known cable length for which the overall channel is equalized.

Examples of ALBO-type equalizers are described in: "Transmission Systems for Communication", Bell Telephone Laboratories, Fourth Edition 1970, pp. 654-655, and in US Patent 5 455 843 to Cherubini et al., entitled "Adaptive Equalizing Apparatus and Method for Token Ring Transmission System Using Unshielded Twisted Pair Cables". The patent discloses an analog equalizer and an associated method to adaptively adjust the equalizer transfer characteristic for a distance between stations that can typically extend up to 200 m. For this range, the attenuation of unshielded twisted pair (UTP) cables is about 10 - 12 dB/100 m at 16 MHz so that the channel attenuation at 16 MHz varies between 0 and 24 dB. The disclosed equalization method is limited to a specific application and cabling structure which makes the disclosed solution unsuitable to cope with the objects of the present invention. In present day cable systems, an ALBO-type equalizer can be realized as a single monolithic semiconductor chip, such as the serial data receiver LIU-01 by Precision Monolithics Inc.

In a paper entitled "Equalizer, Gain, and Timing Control in a Receiver for Multi-level Partial-Response Signals", in the Proceedings of the Fifth Tirrenia International Workshop on Digital Communications, Elsevier Science Publishers B.V., 1992, Cherubini and Ungerboeck describe the adjustment of a two-parameter equalizer consisting of a variable analog filter section and a variable gain amplifier, as well as the adjustment of the sampling phase of an A/D converter in the front-end of a receiver for multi-level PRIV transmission. In the described device, a first control voltage adjusts the variable filter section and a second control voltage determines the front-end gain. The control voltages are derived from the digital output signals of the A/D converter.

The design of a two-parameter equalizer as well as fixed transmit and receive filter sections for PRIV systems was described by G. Cherubini, S. Oelcer, and G. Ungerboeck in "Optimum Filter Design for Partial-Response Class-IV Transmission Systems", Proc. IEEE Intl. Conf. on Communications, ICC '92, pp. 51-56, Chicago, IL, USA, June 1992.

However, an ALBO-type equalizer cannot adequately compensate for the signal distortion if large deviations from the assumed values occur. In this case, signal equalization can be performed - either partially or entirely - by digital filtering. A tutorial treatise on adaptive digital equalization can be found in: E. A. Lee and D. G. Messerschmitt: "Digital Communication", Kluwer Academic Publishers, Boston, MASS, USA, 1988, Ch. 9.

For the present invention, decision-feedback equalization is considered. A digital decision-feedback equalizer (DFE) consists of a linear forward digital filter and a feedback digital filter where past decisions are employed to compute the filter output. Initial convergence of the DFE coefficients to their optimum values is traditionally achieved by reference-directed training where a symbol sequence known to the receiver is sent prior to transmitting the data. When a training sequence is not available, initial DFE convergence must be achieved in a self-training mode.

Self-training adaptive linear equalization for full-response systems was described, e.g., by D.N. Godard in "Self-recovering equalization and carrier tracking in two-dimensional data communication systems", IEEE Trans. Commun., Vol. COM-28, pp. 1867-1875, Nov. 1980, by S. Bellini in "Bussgang techniques for blind equalization", Proc. of IEEE Globecom 1986, pp. 46.1.1 - 46.1.7 , Dec. 1986, and by G. Picchi et al. in "Blind equalization and carrier recovery using a "Stop-and-Go" decision directed algorithm", IEEE Trans. Commun., Vol. COM-35, pp. 877- 887, Sept. 1987. For partial-response systems, self-training adaptive linear equalization was described by Y. Sato in "A method of self-recovering equalization for multilevel amplitude-modulation systems", IEEE Trans. Commun., Vol. COM-23, pp. 679-682, June 1975, and by G. Cherubini, S. Oelcer, and G. Ungerboeck in "Adaptive equalization for PRIV transmission systems", PCT International Patent Application, Publication Number WO 96/20551.

To achieve near maximum-likelihood sequence detection of signals in the presence of intersymbol interference (ISI), the feedback filter of a DFE can be embedded in a Viterbi decoder, as described by A. Duel-Hallen and C. Heegard in "Delayed decision-feedback equalization", IEEE Trans. Commun., Vol. COM-37, pp. 428-436, May 1989, and by M.V. Eyuboglu and S.U. Qureshi in "Reduced-state sequence estimation for coded modulation on intersymbol interference channel", IEEE Trans. Commun., Vol. COM-37, pp. 989 -995, Aug. 1989. The implementation of a Viterbi decoder for partial-response signals was described by S. Oelcer and G. Ungerboeck in "Difference-metric Viterbi decoding of multilevel class-IV partial-response signals", IEEE Trans. Commun., Vol. COM-42, pp. 1558 -1570, Apr. 1994.

Digital equalization for partial-response systems leads to difficulties in connection with timing recovery. The problem arises from the fact that random time continuous PR signals are band-limited to half of the modulation rate. Hence, they are wide-sense stationary. This rules out timing recovery schemes based on cyclo-stationarity, as described by E.A. Lee and D.G. Messerschmitt, cited above, pp. 560-571. Schemes based on signal squaring and tracking a spectral line at

f=1/$T$ Hz, or observing signal transitions cannot be applied. Timing synchronization is usually accomplished by decision-aided schemes. A decision-directed timing recovery scheme that can be applied to full- and partial-response systems was described by K. H. Mueller and M. Muller in "Timing recovery in digital synchronous data receivers", IEEE Trans. Commun., Vol. COM-24, pp. 516-531, Sept. 1976. However, with the Mueller/Muller algorithm, undesirable false-lock situations can be experienced during initial timing acquisition. Conversely, without recovered synchronization, adjustment of a self-training digital adaptive equalizer is possible only by resorting to methods that require considerable complexity and power consumption, as described by Cherubini, Oelcer, and Ungerboeck in "Adaptive equalization for PRIV transmission systems", cited above.

In many applications, transceiver power consumption is not subject to particularly tight constraints. For example, transceivers employed in adapter cards installed in personal computers or the like have usually sufficient power available. However, as will be described, there are also situations where power is a scarce resource, which imposes that the employed transceivers operate with minimal power consumption. This is the case, for example, for LANs deployed outside of buildings where the various devices connected to the network are battery-operated. Under such conditions, precise power management is required.

## OBJECTS OF THE INVENTION

Based on the above, it is one object of the present invention to devise a method for timing recovery in a receiver for high-speed data transmission, which method avoids false-lock situations during initial timing acquisition; it is also an object to design a receiver implementing this method. A further object is to devise a method and a receiver providing robustness against various channel impairments and be tolerant of inaccuracies present particularly in the analog receiver sections. Another object is to devise methods and apparatus to allow a receiver in a full-response or a partial-response system to be able to acquire initial convergence of its parameters

for timing recovery and decision-feedback equalization using received random data signals only, i.e. without the need for a reference-directed start-up procedure. It is a still further object to show a low power implementation which includes the variable linear forward equalizer of the decision-feedback equalizer (DFE) in the analog front-end of a receiver.

## SUMMARY OF THE INVENTION

The solution to these objects consists in employing, in the receiver, a novel timing recovery scheme, preferably in connection with novel approaches for self-training decision-feedback equalization to be applied to full or partial-response transmission systems. Details of these solutions are given in the appended detailed description of a first implementation of the invention in a four-level PRIV system for data transmission over UTP cables, and in a second implementation in a full-response system. However, the principles and concepts of the disclosed receiving techniques are not limited to data transmission over UTP cables but can as well be applied, with appropriate modifications obvious to a person skilled in the art, for data transmission over other types of channels, e.g., magnetic recording channels. The invention addresses two different issues. First, it solves the problem of timing recovery. With this novel scheme, false-lock situations that can be experienced during initial timing acquisition are avoided. Second, it solves the problem of initial DFE convergence by implementing a self-training linear forward equalizer, for which convergence can be achieved using received random data signals, and a feedback filter with small adaptivity.

The solution according to the invention for a quaternary PRIV system shows the linear forward equalizer realized as a self-training two-parameter variable analog filter. Two-parameter variable equalizer adjustment for partial-response systems goes back to the theoretical principle explained by Cherubini and Ungerboeck in "Equalizer, Gain, and Timing Control in a Receiver for Multilevel Partial-Response Signals", cited above. The linear forward equalization by a variable analog filter

leads to the advantage of low power consumption. After synchronization has been accomplished, convergence of the digital feedback filter embedded in a reduced-state Viterbi decoder is achieved. This approach leads to an implementation with low complexity that permits to reduce power consumption even further. The small adaptivity provided by the Viterbi decoder allows compensating for the residual signal distortion at the output of the analog linear forward equalizer and ensures correct convergence of the feedback filter coefficients to their optimum values without the need for a training sequence.

The solution according to the invention for a full-response system shows the linear forward equalizer realized as a self-training adaptive digital filter. The algorithm employed for self-training equalization is an inventive extension to full-response systems of the algorithm for partial-response systems described by Cherubini, Oelcer, and Ungerboeck in "Adaptive equalization for PRIV transmission systems", cited above. As in the case of PR systems, convergence of the feedback filter coefficients to their optimum values takes place without the need for a training sequence after timing recovery and convergence of the linear forward equalizer have been accomplished.

## LIST OF DRAWINGS

Fig.1 shows an overview of the system in which the invention is used;
Fig.2 illustrates a connection between two nodes in the system according to Fig.1;
Fig.3 depicts a first embodiment, a transceiver in a partial-response system;
Fig.4 illustrates the computation of the timing control signal;
Fig.5 shows a second embodiment, a transceiver in a full-response system.

## DETAILED DESCRIPTION

Fig.1 provides a simplified overview of a system which makes advantageous use of the invention, a system developed for seismic data acquisition. A backbone network connects router units (RUs) 2 via bi-directional high-speed fiber links 3 to a central system 1. Ground networks connect signal processing units (SPUs) 6 via bi-directional cable links 4 to the RUs. Each SPU 6 can receive analog signals from a plurality of geophones 7, digitize these signals, and send them upstream to central system 1. In addition, each SPU 6 receives and transmits control and status information.

Fig.2 illustrates the communication arrangement between two adjacent SPUs 6. The SPU functions are controlled by a controller 8 which interfaces with two transceivers 9 designated T1 and T2. In the embodiment, each transceiver 9 supports full-duplex transmission at a nominal rate of 16 Mbit/s, and at a fallback rate of 8 Mbit/s. The cable links 4 connecting two SPUs contain unshielded twisted-pair cables 11 for digital transmission, and additional pairs 10 over which analog signals from geophones 7 (shown in Fig.1) are received and digitized by converter 5. Power consumption for simultaneous transmit and receive operation is less than 200 mW from a single 3.3V supply voltage.

The characteristics of the cables used for the cable links 4 are specified as follows:

- 30 dB signal attenuation at 4 MHz for maximum cable length,
- 55 dB near-end crosstalk attenuation at 4 MHz, and
- a characteristic impedance of 108 +/- 15 Ohm.

The two transceivers 9 shown schematically in Fig.2 are controlled via a common microcontroller which permits setting of transceiver options, e.g. quaternary transmission or binary transmission (as a fallback), and reading of receiver parameters, e.g. mean squared-error at the detection point of each receiver.

In the following, a more detailed description of a transceiver 9 and its functions shall be given. The transceiver design is based on quaternary partial-response class-IV (QPRIV) signaling.

With QPRIV modulation, quaternary symbols $a_n \in \{-3,-1,+1,+3\}$ are transmitted. The signals at the output of the overall discrete-time channel are shaped into the form $x_n = a_n - a_{n-2} + e_n$, where $e_n$ accounts for residual distortion and noise. Note that the output of an ideal QPRIV system is a sequence of signals from the set { -6, -4, -2, 0, +2, +4, +6 }.

The overall channel characteristic exhibits spectral nulls at 0 Hz and the bandedge frequencies of $\pm 1/2T$ Hz, where $1/T$, here 8 MBaud, is the modulation rate. Hence, transmitted signal energy is greatly reduced at low frequencies, where the transfer function of the cable varies rapidly with frequency, and at high frequencies, where signals become more attenuated. Channel equalization can thus be accomplished more easily than for full-response signaling and partial-response class-I signaling (PRI) with spectral nulls only at $\pm 1/2T$

Fig.3 gives an overview of one single transceiver incorporating the invention. Each transceiver consists of a digital section 12, in which digital signal processing functions are performed, and a front-end section 13 for signal conversion, analog filtering, receiver clock generation, and cable driver/receiver functions.

In the transmitter, incoming quaternary symbols are represented by a 2-bit signal TDAT. These incoming information bits are scrambled in self-synchronizing scrambler 14 using the scrambler polynomial $1+D^{13}+D^{28}$ and encoded by a 2B1Q differential encoder 15 to achieve transparency with respect to received signal polarity. After 2-bit digital-to-analog conversion in D/A converter 16, the resulting signal is shaped by a fixed transmit filter 17 into approximate PRIV form, then amplified by power amplifier 18, and transmitted via cable 11.

An incoming signal - from cable 11 - is amplified by variable gain amplifier (VGA) 19 and shaped into PRIV form by an analog receive filter consisting of a variable filter section 20 and a fixed filter section 21. Two independent control voltages determine the adjustments carried out by the variable equalizer: one voltage determines the frequency-independent gain of VGA 19, the other voltage controls the transfer characteristic of variable filter 20. The control signals for the variable equalizer are derived digitally in a manner that leads to optimum settings independently of the current sampling phase.

Received signal samples $x_n$ are obtained in analog-to-digital (A/D) converter 22 by 6-bit A/D conversion at a rate equal to $1/T$ symbols per second. The sampling phase of A/D converter 22 is determined by a voltage-controlled oscillator (VCO) 23 whose control voltage is adjusted by a decision-directed timing recovery algorithm. For proper operation of the timing recovery algorithm, a sufficient degree of equalization has to be achieved by the sampling-phase insensitive equalizer control method. To simplify conversion, the control voltage for VCO 23 is provided by control circuit 29 in binary sigma-delta modulated form, as are the control voltages for VGA 19 and the variable filter section 20. A bank of three sigma-delta demodulators 24 to 26 serves to derive the required analog control voltages.

The thus obtained 6-bit-wide digital signal samples are input to an adaptive reduced two-state Viterbi decoder, element 27, for maximum-likelihood sequence detection. Embedded in this Viterbi decoder is the adaptive feedback filter of a decision-feedback equalizer (DFE) to remove residual intersymbol interference. Symbol-by-symbol detection can also be employed. In this case, element 27 consists of a memory-less decision element and a feedback filter.

An estimate of the average squared error signal (MSE) is computed in an MSE meter 28. The MSE and other digital section receiver parameters may be used to allow monitoring of a "transmission-link quality". The signals at the output of the Viterbi decoder are differentially decoded and descrambled in descrambler 30. The

recovered quaternary symbols are represented by the two-bit signal RDAT at the output of the digital section 12 of the transceiver.

Light line 31 in Fig.3 carries a receiver clock signal RCLK produced by VCO 23; this clock signal RCLK controls all digital receiver functions. In the transmit section of the transceiver, an externally provided transmitter clock signal TCLK serves the same function, as indicated.

The transceiver, as implemented, comprises a digital chip and a mixed analog/digital chip; it further includes various external components, such as analog filters, transformers, oscillator crystal, etc., which are not shown in detail; a person skilled in the art will be able to implement them. The digital chip performs the required digital signal processing functions and also incorporates a microcontroller interface. The mixed analog/digital chip performs the functions of D/A conversion and power amplification required for the transmit section of the transceiver front-end and the functions of variable gain amplification, signal buffering and A/D conversion needed for the receive section. Fixed passive analog filters for signal shaping are realized as a hybrid module. Analog signal equalization capability is provided by an external variable filter section. The variable elements of the variable filter can be realized, for example, by employing a matched n-channel JFET pair. As mentioned above, receiver timing is provided by VCO 23, which is here implemented as a voltage-controlled crystal oscillator.

The main features of the transceiver as implemented for a LAN for seismic data acquisition, are:

- Transmission at 16 Mbit/s up to 250 m of voice-grade cable (UTP3) and up to 400 m of data-grade cable (UTP5);
- Fall-back rate of 8 Mbit/s (binary transmission);
- Power consumption of 200 mW at single +3.3 V operation voltage;
- Operating temperature from -50°C to +85°C;
- Link quality monitoring capability.

The following is a more detailed description of the control functions as implemented in the above device. Variable gain, variable analog filter section, and timing are adjusted in the receiver's front end by three control voltages:

- control voltage $u_{VGA}$ determines a frequency-independent gain of amplifier 19,
- control voltage $u_{EQZ}$ varies the transfer function of the variable filter section 20,
- control voltage $u_{VCO}$ controls the frequency of the voltage-controlled oscillator 23 and thus the sampling phase $t_s$ of A/D converter 22. The adjustments for these control voltages are computed in the digital transceiver section 12 by the following algorithms.

**Gain Control**

The value $u_{VGA,n}$ stored in a digital accumulator of the VGA control loop at time $n$ is adjusted according to the algorithm

$$u_{VGA,n+1} = u_{VGA,n} - \alpha_G \Delta u_{VGA,n}, \quad 0 < \alpha_G << 1,$$

where $\alpha_G$ is the adaptation gain, and

$$\Delta u_{VGA,n} = x_n^2 - 2\sigma_a^2,$$

where $\sigma_a^2 = E\{a_n^2\}$ denotes the variance of the channel input symbols.

For a low-complexity implementation, the adjustment term $\Delta u_{VGA,n}$ can be computed so that the A/D converter output signal samples achieve the same probability distribution as an ideal QPRIV signal:

$$\Delta u_{VGA,n} = \begin{cases} -7 & \text{if } x_n \geq 6 \\ 1 & \text{if } x_n \leq 2 \\ 0 & \text{if otherwise.} \end{cases}$$

The value $u_{VGA,n}$ is then converted into a single-bit control signal by first-order sigma-delta demodulation, not described here.

**Adaptive Analog Equalizer Control**

For an ideal PRIV signal $x_{PRIV}(t)$, the autocorrelation function

$$R_{xx,PRIV}(t') = E\{x_{PRIV}(t)\, x_{PRIV}(t+t')\}$$

vanishes at $t' = T$.

Since $\Delta u_{EQZ,n} = x_n x_{n-1}$ represents an unbiased estimate of $R_{xx}(T)$, the value $u_{EQZ,n}$ stored in a digital accumulator of the equalizer control loop is adjusted according to the algorithm:

$$u_{EQZ,n+1} = u_{EQZ,n} - \alpha_E \Delta u_{EQZ,n}, \quad 0 < \alpha_E << 1,$$

wherein $\alpha_E$ is an adaptation gain. The value $u_{EQZ,n}$ is then converted into a single-bit control signal by first-order sigma-delta demodulation, not described here.

**Timing Control**

In a decision-directed timing recovery algorithm, the sampling phase adjustment $\Delta\tau_n$ is computed to minimize the mean-square value of the error signal $e_n = x_n - s_n$, where $s_n$ denotes the signal sample at the output of an ideal channel at time $n$. The stochastic gradient of $E\{(x_n - s_n)^2\}$ with respect to the sampling phase $t_S$ is proportional to $(x_n - s_n)\dot{x}_n \approx (x_n - s_n)(x_{n+1} - x_{n-1})$, wherein $\dot{x}_n$ is a time derivative of $x_n$. This leads to the definition of the gradient given by Muller and Mueller:

$$\nabla_\tau(e_n^2) \approx \hat{e}_n (x_{n+1} - x_{n-1}) = \Delta\tau_n^{MM},$$

where $\hat{e}_n = x_n - \hat{s}_n$ is an estimate of the error signal obtained from a tentative decision $\hat{s}_n$ on the symbol $s_n$. However, using the above gradient has the disadvantage that the S-curve of the timing recovery loop, which is defined as the expectation of the gradient as a function of the sampling phase, exhibits a behavior that might determine false-lock situations during initial timing acquisition. To overcome such difficulty, a modified Muller-Mueller algorithm is adopted, where the gradient is given by

$$\nabla_\tau(e_n^2) \approx \hat{e}_n \left(\hat{s}_n\right)^2 (x_{n+1} - x_{n-1}) = \Delta\tau_n.$$

This signal is then input to a second-order loop filter. The filter output $\Delta\tau_{s,n}$ and a value $u_{acc,n}$, stored in the accumulator of the loop filter, are computed as follows:

$$\Delta\tau_{s,n} = u_{acc,n} + \gamma\,\Delta\tau_n, \qquad u_{acc,n+1} = u_{acc,n} + \zeta\,\Delta\tau_n$$

wherein $\gamma$ and $\zeta$ are suitably selected loop gains. The value $\Delta\tau_{s,n}$ is then converted into a single-bit control signal by first-order sigma-delta demodulation, not described here.

To simplify the realization of the modified Muller-Mueller timing recovery algorithm, an approximation of the term $(\hat{s}_n)^2$ can be employed. Fig.4 shows the block diagram of a simplified realization for a QPRIV system, where

$$\Delta\tau_n = \begin{cases} 2\,\hat{e}_n\,(x_{n+1} - x_{n-1}) & \text{if } |\hat{s}_n| = 6 \\ \hat{e}_n\,(x_{n+1} - x_{n-1}) & \text{if } |\hat{s}_n| = 4 \\ 0 & \text{otherwise.} \end{cases}$$

**Viterbi Decoder with Embedded Feedback Filter**

The received signal, denoted by $x_n$, is given by

$$x_n = \sum h_l a_{n-l} + \text{noise.}$$

Since signal shaping into PRIV form is approximately achieved by analog equalization, one can assume for the system impulse response $\{h_l\}$: $h_0 \approx +1$, $h_2 \approx -1$, and $h_l \approx 0$, $l \neq 0,2$. Hence, one can rewrite the expression for the signal $x_n$ as

$$x_n = (+1 + \Delta h_0)a_n + (-1 + \Delta h_2)a_{n-2} + \sum_{l=1,\, l\neq 2}^{9} \Delta h_l a_{n-l} + \text{noise,}$$

where it is assumed that $h_l = 0$ for $l < 0$ and $l > 9$.

A simplified Viterbi decoding algorithm for the signal $x_n$ is described as follows. The received signal is first adjusted by removing the contribution of the intersymbol interference term $\sum_{l=1,l\neq 2}^{9} \Delta h_l a_{n-l}$. An estimate of this term is provided by an auxiliary feedback filter in element 27 that uses tentative symbol decisions

$$\hat{a}'_{n-1}, \hat{a}'_{n-3}, \hat{a}'_{n-4} \ldots \hat{a}'_{n-9},$$

from the most likely Viterbi decoder survivor path. The resulting signal is given by

$$\tilde{x}_n = x_n - \sum_{l=1,l\neq 2}^{9} \Delta\hat{h}_{l,n}\ \hat{a}'_{n-l}$$

where $\Delta\hat{h}_{l,n}$ represents an estimate of the coefficient $\Delta h_l$ at time $n$.

The Viterbi decoder operates on the signals $\{\tilde{x}_n\}$ and determines the symbol sequence $\{\hat{a}_n\}$ which minimizes

$$\sum_n \left[ \tilde{x}_n - (+1 + \Delta \hat{h}_{0,n}) \hat{a}_n - (-1 + \Delta \hat{h}_{2,n}) \hat{a}_{n-2} \right]^2 = \sum_n \hat{e}_n^2 .$$

The estimates of the channel impulse responses $\Delta\hat{h}_{0,n}, \Delta\hat{h}_{1,n}, \ldots\ldots\Delta\hat{h}_{9,n}$ are determined by an adaptive LMS algorithm such as to minimize $\sum_n \hat{e}_n^2$ .

To reduce implementation complexity, reduced-state Viterbi decoding is employed. State reduction is achieved by grouping the two states corresponding to the symbols +3 and -1 into one single state, and by grouping the two states corresponding to the symbols +1 and -3 into a second state. Note that state reduction requires that parallel transitions are resolved prior to the computation of the branch metrics. In order to reduce propagation delay, parallel transitions are resolved using the signal $x_n$ rather than $\tilde{x}_n$ . This approach is justified by our earlier assumption that the channel impulse response does not significantly deviate from the impulse response of an ideal PRIV channel. Note also that since at any time instant only two states are retained, the difference of the survivor metrics can be propagated from one iteration to the next, rather than the survivor metrics themselves.

A block diagram with the main functions of the adaptive Viterbi decoder with auxiliary feedback filter can be developed by someone skilled in the art. In an adaptive survivor metric unit, the difference metric is iteratively computed, the extension of the survivor sequences is determined, and the estimates $\Delta \hat{h}_{0,n}$ and $\Delta \hat{h}_{2,n}$ are obtained by an adaptive LMS algorithm. A path history unit is used to store the two survivor sequences. An adaptive auxiliary feedback filter computes the signal correction term

$$\sum_{l=1,\ l\neq 2}^{9} \Delta \hat{h}_{l,n}\ \hat{a}'_{n-l}$$

using tentative symbol decisions stored in the path history unit, and adaptively generates the estimates $\Delta \hat{h}_{1,n}$ , $\Delta \hat{h}_{3,n}$ , ..... , $\Delta \hat{h}_{9,n}$ . No detailed implementations of the adaptive survivor metric unit, the path memory, and the adaptive auxiliary feedback filter are shown since these can be implemented by someone skilled in the art.

**Mean-Squared Error Computation**

The mean-squared error is computed in MSE meter 28 by low-pass filtering the metric increments. Such a device, again, can be implemented by someone skilled in the art and need therefore not be shown here in detail.

**Descrambler and Differential Decoder**

The bits representing the symbols output by the Viterbi decoder 27 are differentially decoded and descrambled by descrambler 29 which includes a descrambler whose transfer function is given by $(1 + D^{13} + D^{28})$. The descrambler output signal represents the recovered information bits. This concludes the description of the partial-response system.

**Full-Response System**

An embodiment of the invention for a quaternary full-response system is shown in Fig.5 and described in the following. The filtering elements at the transmitter and the receiver must ensure that the signal $y_n$ obtained at the decision element of an adaptive digital equalizer 57, in the embodiment a DFE, is free from intersymbol interference. This signal is given by $y_n = a_n +$ noise, where $a_n \in \{-3, -1, +1, +3\}$ for quaternary modulation. In the embodiment, the linear forward equalizer of the DFE is realized by a digital transversal filter.

Fig.5 gives an overview of a transceiver incorporating a full-response embodiment according to the invention. Each transceiver consists of a digital section 42, in which digital signal processing functions are performed, and a front-end section 43 for signal conversion, analog filtering, receiver clock generation, and cable driver/receiver functions.

In the transmitter, incoming quaternary symbols are represented by a 2-bit signal TDAT'. These incoming information bits are scrambled in scrambler 44 using the polynomial $1 + D^{13} + D^{28}$ and encoded by a 2B1Q differential encoder 45 to achieve transparency with respect to received signal polarity. After 2-bit digital-to-analog

conversion in D/A converter 46, the resulting signal is shaped by a fixed transmit filter 47, then amplified by power amplifier 48, and transmitted via cable 41.

An incoming signal - from cable 41 - is amplified by variable gain amplifier (VGA) 49 and filtered by a fixed analog filter 51. A control voltage determines the frequency-independent gain of VGA 49. The control signal for the VGA is derived digitally.

Received signal samples $x_n$ are obtained in analog-to-digital (A/D) converter 52 by 6-bit A/D conversion at a rate of $1/T$ symbols per second. The sampling phase of A/D converter 52 is determined by a voltage-controlled oscillator (VCO) 53 whose control voltage is adjusted by the disclosed decision-directed timing recovery algorithm. To simplify conversion, the control voltage for VCO 53 is provided by control circuit 59 in binary sigma-delta modulated form, as is the control voltage for VGA 49. Two sigma-delta demodulators 54 and 56 serve to derive the required analog control voltages.

**Self-Training Equalization for Full-Response Systems**

The thus derived 6-bit-wide signal samples $x_n$ are transferred into the delay line of the linear forward equalizer of an adaptive equalizer 57, here a decision feedback equalizer (DFE). The output of this equalizer is given by

$$y_n = \underline{c}_n^T \underline{x}_n - \underline{d}_n^T \underline{\hat{a}}_n ,$$ wherein

$\underline{c}_n^T = \{c_{0,n}, \ldots, c_{N-1,n}\}$ denotes the vector of coefficients of the linear forward equalizer,

$\underline{d}_n^T = \{d_{1,n}, \ldots, d_{L-1,n}\}$ denotes the vector of coefficients of the feedback filter,

$\underline{x}_n^T = \{x_n, \ldots, x_{n-N+1}\}$ represents the vector of signals stored in the equalizer delay line at time $n$, and

$\underline{\hat{a}}_n^T = \{\hat{a}_{n-1}, \ldots, \hat{a}_{n-L+1}\}$ represents the vector of tentative quaternary decisions stored in the feedback filter delay line at time $n$.

Traditionally, the LMS algorithm described in E. A. Lee, and D. G. Messerschmitt, cited above, Ch. 9, is employed for decision-directed adjustment of the DFE coefficients:

$$\underline{c}_{n+1} = \underline{c}_n - \alpha_{dd}\, \hat{e}_n\, \underline{x}_n,$$
$$\underline{d}_{n+1} = \underline{d}_n + \alpha_{dd}\, \hat{e}_n\, \underline{\hat{a}}_n,$$

where $\alpha_{dd}$ is the adaptation gain and $\hat{e}_n$ an error signal given by $\hat{e}_n = y_n - \hat{a}_n$.

If the DFE operates in self-training mode, the coefficients of the feedback filter are normally set to zero; then the output of the equalizer is given by $y_n = \underline{c}_n^T\, \underline{x}_n$.

For self training, we cannot rely on the correctness of decisions $\underline{\hat{a}}_n$, and hence on the error signals $\hat{e}_n$. We will use instead of $\hat{e}_n$ a pseudo error defined by

$$\varepsilon_n = \begin{cases} y_n - \hat{a}_n & \text{if } |y_n| \geq 3 \\ -\delta_n\, sign(y_n) & \text{otherwise,} \end{cases}$$

where $\delta_n$ is a parameter in the range $(0, \delta_{max})$, $\delta_{max} > 0$. The parameter is updated at each iteration as follows:

$$\delta_{n+1} = \begin{cases} \delta_n - 3\Delta & \text{if } |y_n| \geq 3, \\ \delta_n + \Delta & \text{otherwise,} \end{cases}$$

and $\Delta$ is a small positive constant

The generation of the pseudo error $\varepsilon_n$ is based on a priori knowledge of the statistics of the signal. In the case of accomplished equalization, $y_n$ corresponds to the quaternary channel input symbols $a_n$ embedded in noise. Therefore, whenever the event $|y_n| \geq 3$ is observed, we can use $y_n - \hat{a}_n$ as a trusted error to update the equalizer coefficients. If we observe the event $|y_n| < 3$, no trusted error is available. In this case, we choose to update the equalizer coefficients so that the probabilities of the events $|y_n| < 3$ and $|y_n| \geq 3$ assume the values 3/4 and 1/4 , respectively, which are the probabilities of these events for an ideally equalized noisy quaternary signal, provided that the input symbols form a sequence of independent identically distributed random variables. This is achieved by setting the pseudo error equal to $\delta_n\, sign(y_n)$ whenever $|y_n| < 3$ and updating the value of $\delta_n$ at each iteration so that $\delta_n$ becomes larger if the event $|y_n| < 3$ occurs more often than expected, and $\delta_n$ becomes smaller otherwise.

The algorithm for self-training adaptive equalization is then given by

$$\underline{c}_{n+1} = \underline{c}_n - \alpha_{st}\, \varepsilon_n\, \underline{x}_n ,$$

where $\alpha_{st}$ is the adaptation gain during self training.

Several variants of the algorithm can be obtained through different simplifications. For example, pseudo errors can be computed based on the signal energy at the equalizer output. If the signal energy is found to be too often below a given threshold, the error term is set equal to $-c\, sign(y_n)$, where $c$ is a positive constant, whenever $|y_n| < 3$, and trusted errors are used when $|y_n| \geq 3$.

In this embodiment, symbol-rate sampling at the receiver is assumed . In practice, it is common to sample the received signal at a rate larger than the symbol rate and employ fractionally-spaced equalization. The extension of the described self-training algorithm to this case is straightforward.

An estimate of the average squared error signal (MSE) at the decision point is computed in MSE meter 50 to monitor the "transmission-link quality". If the MSE drops below a given threshold, tentative decisions on the transmitted symbols are sufficiently reliable. Then the DFE enters decision-directed mode and updating of all DFE coefficients by the LMS algorithm takes place.

As an alternative to the above described freezing the coefficients of the feedback filter in the self-training mode, these coefficients can be updated also during self training by $\underline{d}_{n+1} = \underline{d}_n + \alpha_{st}\, \varepsilon_n\, \underline{\hat{a}}_n$.

The signals at the output of the decision feedback filter are differentially decoded and descrambled in descrambler 60. The recovered quaternary symbols are represented by the two-bit signal RDAT at the output of the digital section 42 of the transceiver.

Light line 61 in Fig.5 carries a receiver clock signal RCLK' produced by VCO 53; this clock signal RCLK' controls all digital receiver functions. In the transmit section of the transceiver, an externally provided transmitter clock signal TCLK' serves the same function, as indicated.

The invention has been shown and explained with reference to the drawings and the underlying theoretical considerations; these details, however, are not intended to limit the scope of the invention as defined in the appended claims.

CLAIMS

1. A method for achieving timing recovery in a receiver of a digital communication system,

characterized by controlling the sampling time of an analog/digital converter (22, 52) in said receiver by means of a gradient defined as

$$g_1(\hat{e}_n)\, g_2(\hat{s}_n)(x_{n+1} - x_{n-1})$$

wherein $x_n$ is the signal sample at the output of said converter (22, 52) at time $n$, $\hat{e}_n$ is an error term given by $\hat{e}_n = x_n - \hat{s}_n$, $\hat{s}_n$ being a tentative decision on the received signal, $g_1(\hat{e}_n)$ is a function of said error term, and $g_2(\hat{s}_n)$ is a function of said tentative decision.

2. The method of claim 1, wherein the function $g_1(\hat{e}_n)$ is defined as $g_1(\hat{e}_n) = \hat{e}_n$.

3. The method of claim 1, wherein the function $g_2(\hat{s}_n)$ is defined as $g_2(\hat{s}_n) = |\hat{s}_n|^m$, $m$ being larger than 1, preferably at least 2.

4. A method for detecting and recovering signals in a receiver of a communication system with a timing recovery scheme according to any of claims 1 to 3, adapted for partial-response transmission, said receiver including a variable gain amplifier (19), a variable filter (20), and the analog/digital converter (22), characterized by

- forming an estimate of the time-discrete autocorrelation function $R_{xx}(t')$ of a received signal, the value of said function for $t' = kT$ being given by the expected value of the product of the signal samples taken at the output of said analog/digital converter (22) at time $t$ and at time $t+kT$, $T$ being the modulation interval,

- controlling said variable gain amplifier (19) by a first value being derived from said estimate of the time-discrete autocorrelation function $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = 0$,

- controlling said variable filter (20) by a second value being derived from said estimate of the time-discrete autocorrelation function $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = T$.

5. Apparatus for detecting and recovering received signals in a partial-response communication system, said apparatus including a variable gain amplifier (19), a variable filter (20) and an analog/digital converter (22), further comprising

- means (29) for producing an estimate of the time-discrete autocorrelation function $R_{xx}(t')$ of a received signal, the value of said estimate for $t' = kT$ being given by the product of a digital signal sample taken at the output of said analog/digital converter (22) at time $t$ with a signal sample taken at time $t+kT$,

- means (26, 29) for controlling the gain of said amplifier (19) by a first voltage being derived from a first value of said estimate of $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = 0$,

- means (25, 29) for controlling the transfer characteristics of said variable filter (20) using a second voltage being derived from a second value of said estimate of $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = T$, and

- means (23, 24, 29) for controlling the sampling time of said analog/digital converter (22) by a third voltage being derived according to the timing recovery method of any of the claims 1 to 3.

6. A method for detecting and recovering signals in a partial response communication system with a timing recovery scheme according to any of the claims 1 to 3, said receiver including a variable gain amplifier (19), a variable analog forward filter (20), an analog/digital converter (22), and a component (27) with a decision element and an adaptive feedback filter, altogether forming a "decision feedback

equalizer" (DFE), the method comprising, for achieving initial DFE convergence in a self-training mode,

- forming an estimate of the time-discrete autocorrelation function $R_{xx}(t')$ of a received signal, the value of said function for $t' = kT$ being given by the expected value of the product of the signal samples taken at the output of said analog/digital converter (22) at time $t$ and at time $t+kT$,

- controlling said variable gain amplifier (19) by a first value being derived from said estimate of the time-discrete autocorrelation function $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = 0$, and

- controlling said variable filter (20) by a second value being derived from said estimate of the time-discrete autocorrelation function $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = T$.

7. The method according to claim 6, wherein the feedback filter is embedded in a Viterbi decoder, preferably a reduced-state Viterbi decoder, for maximum-likelihood sequence detection.

8. Apparatus for detecting and recovering received signals in a partial response communication system, said apparatus including a variable gain amplifier (19), a variable analog forward filter (20), an analog/digital converter (21), and a component (27) including a decision element and an adaptive digital feedback filter, altogether forming a "decision feedback equalizer" (DFE), the apparatus further comprising, for achieving initial DFE convergence in a self-training mode,

- means (29) for producing an estimate of the time-discrete autocorrelation function $R_{xx}(t')$ of a received signal, the value of said estimate for $t' = kT$ being given by the product of a digital signal sample taken at the output of said analog/digital converter (21) at time $t$ with a signal sample taken at time $t+kT$,

- means (26, 29) for controlling the gain of said amplifier (19) by a first voltage, said first voltage being derived from a first value of said estimate of $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = 0$, and

- means (25, 29) for controlling the transfer characteristics of said filter (20) using a second voltage, said second voltage being derived from a second value of said estimate of $R_{xx}(t')$, preferably by a value derived from said estimate at $t' = T$.

9. The apparatus of claim 8, wherein the component (27) includes a Viterbi decoder, preferably a reduced-state Viterbi decoder, with a digital feedback filter embedded in said Viterbi decoder.

10. The method according to any of the claims 4, 6, or 7, wherein the variable gain amplifier (19) is controlled conforming to

$$u_{VGA,n+1} = u_{VGA,n} - \alpha_G \Delta u_{VGA,n}\ ,\ 0 < \alpha_G << 1,$$

$u_{VGA,n}$ being the voltage controlling said variable gain amplifier (19) at time $nT$,
$\alpha_G$ being the adaptation gain, and
$\Delta u_{VGA,n}$ being the adjustment term.

11. The method according to any of the claims 4, 6, or 7, wherein the variable filter (20) is controlled conforming to

$$u_{EQZ,n+1} = u_{EQZ,n} - \alpha_E \Delta u_{EQZ,n}\ ,\ 0 < \alpha_E << 1,$$

$u_{EQZ,n}$ being the voltage controlling said variable filter (20) at time $nT$,
$\alpha_E$ being the adaptation gain, and
$\Delta u_{EQZ,n}$ being the adjustment term.

12. The apparatus of any of the claims 5, 8 or 9, wherein one or more sigma-delta demodulators (24, 25, 26) are provided to derive analog control voltages, the input

to the demodulator (26) associated with the variable gain amplifier (19) being controlled according to

$$u_{VGA,n+1} = u_{VGA,n} - \alpha_G \Delta u_{VGA,n} \ , \ 0 < \alpha_G << 1,$$

$u_{VGA,n}$ determining the voltage controlling said variable gain amplifier (19),
$\alpha_G$ being the adaptation gain,
$\Delta u_{VGA,n}$ being the adjustment term,

and/or the input to the demodulator (25) associated with variable filter (20) being controlled according to

$$u_{EQZ,n+1} = u_{EQZ,n} - \alpha_E \Delta u_{EQZ,n} \ , \ 0 < \alpha_E << 1,$$

$u_{EQZ,n}$ determining the voltage controlling said variable filter (20),
$\alpha_E$ being the adaptation gain, and
$\Delta u_{EQZ,n}$ being the gradient term.

13. A method for detecting and recovering signals in a receiver of a communication system with a timing recovery scheme according to any of claims 1 to 3, adapted for full-response M-ary transmission, said receiver including a variable gain amplifier (49), an analog/digital converter (52), and an adaptive equalizer (57) with a linear forward filter and a decision element, the method comprising, for achieving initial convergence in a self-training mode,

- forming a pseudo-error $\varepsilon_n$ defined by

$$\varepsilon_n = \begin{cases} y_n - \hat{a}_n & \text{if } |y_n| \geq M-1 \\ -\delta_n \, sign(y_n) & \text{otherwise,} \end{cases}$$

where $y_n$ is the output of said equalizer (57), $\hat{a}_n$ is a tentative M-ary decision, and $\delta_n$ is a positive parameter updated at each iteration according to

$$\delta_{n+1} = \begin{cases} \delta_n - \Delta_1 & \text{if } |y_n| \geq M-1 \\ \delta_n + \Delta_2 & \text{otherwise,} \end{cases}$$

$\Delta_1$ and $\Delta_2$ being positive constants,

- updating the vector $\underline{c}_n$ of the coefficients of said linear forward filter according to

$$\underline{c}_{n+1} = \underline{c}_n - \alpha_{st}\, \varepsilon_n\, \underline{x}_n,$$

where $\alpha_{st}$ is the adaptation gain and $\underline{x}_n$ is the vector of signal samples taken at the output of said converter (52).

14. The method according to claim 13, the adaptive equalizer (57) further including a feedback filter,

wherein the vector $\underline{d}_n$ of the coefficients of said feedback filter, for achieving initial convergence in a self-training mode, is updated according to

$$\underline{d}_{n+1} = \underline{d}_n + \alpha_{fb}\, \varepsilon_n\, \underline{\hat{a}}_n,$$

where $\underline{\hat{a}}_n$ is the vector of tentative decisions and $\alpha_{fb}$ is an adaptation gain for the feedback filter which can be either positive or zero.

15. Apparatus for detecting and recovering received signals in a full-response communication system, said apparatus including a variable gain amplifier (49), an analog/digital converter (52), and an adaptive equalizer (57) with a linear forward filter and a decision element, comprising, for achieving initial convergence in a self-training mode, in said adaptive equalizer (57)

- means for forming a pseudo-error $\varepsilon_n$ defined by

$$\varepsilon_n = \begin{cases} y_n - \hat{a}_n & \text{if } |y_n| \geq M-1 \\ -\delta_n\, sign(y_n) & \text{otherwise,} \end{cases}$$

where $\delta_n$ is the output of said equalizer (57), $\hat{a}_n$ is a tentative M-ary decision, and $\delta_n$ is a positve parameter updated at each iteration according to

$$\delta_{n+1} = \begin{cases} \delta_n - \Delta_1 & \text{if } |y_n| \geq M-1, \\ \delta_n + \Delta_2 & \text{otherwise,} \end{cases}$$

$\Delta_1$ and $\Delta_2$ being positive constants,

- means for updating the vector $\underline{c}_n$ of the coefficients of said linear forward filter according to

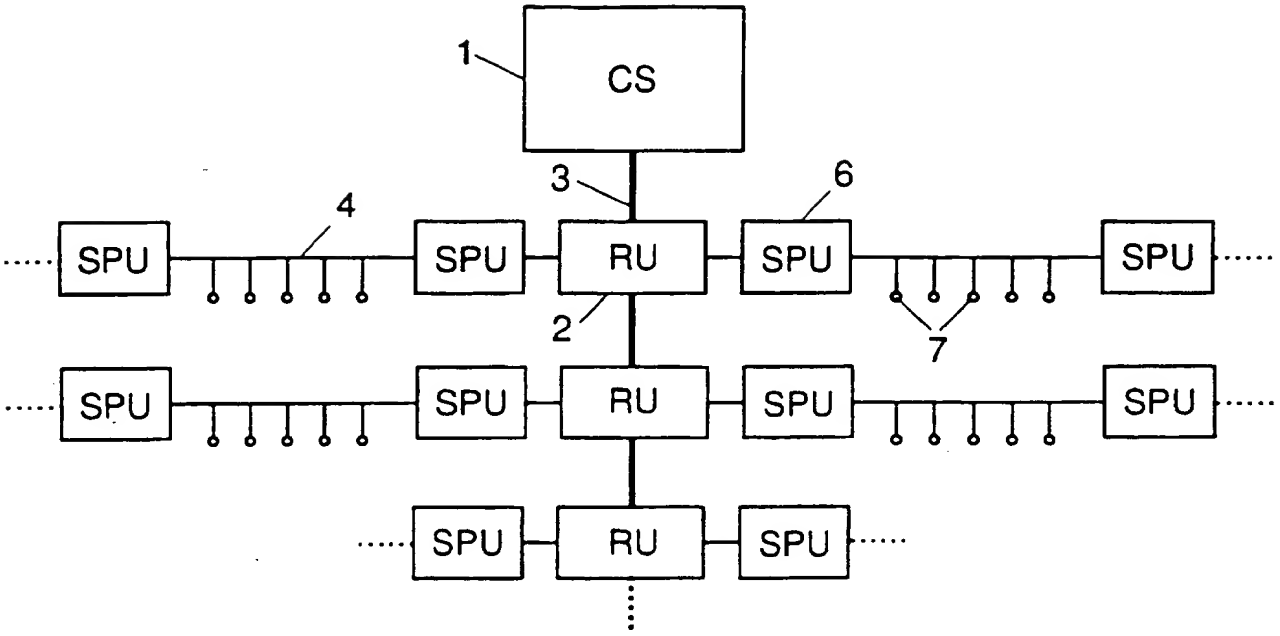
$$\underline{c}_{n+1} = \underline{c}_n - \alpha_{st}\, \varepsilon_n\, \underline{x}_n,$$

where $\alpha_{sl}$ is the adaptation gain and $\underline{x}_n$ is the vector of signal samples taken at the output of said converter (52).

16. The apparatus according to claim 15, the adaptive equalizer (57) further including a feedback filter and means for updating the vector $\underline{d}_n$ of the coefficients of said feedback filter according to

$$\underline{d}_{n+1} = \underline{d}_n + \alpha_{fb}\, \varepsilon_n\, \underline{\hat{a}}_n,$$

where $\underline{\hat{a}}_n$ is the vector of tentative decisions and $\alpha_{fb}$ is an adaptation gain for the feedback filter which can be either positive or zero.


1
CS
3
6
4
SPU
SPU
RU
SPU
SPU
2
7
SPU
SPU
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SPU
SPU
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Fig.1

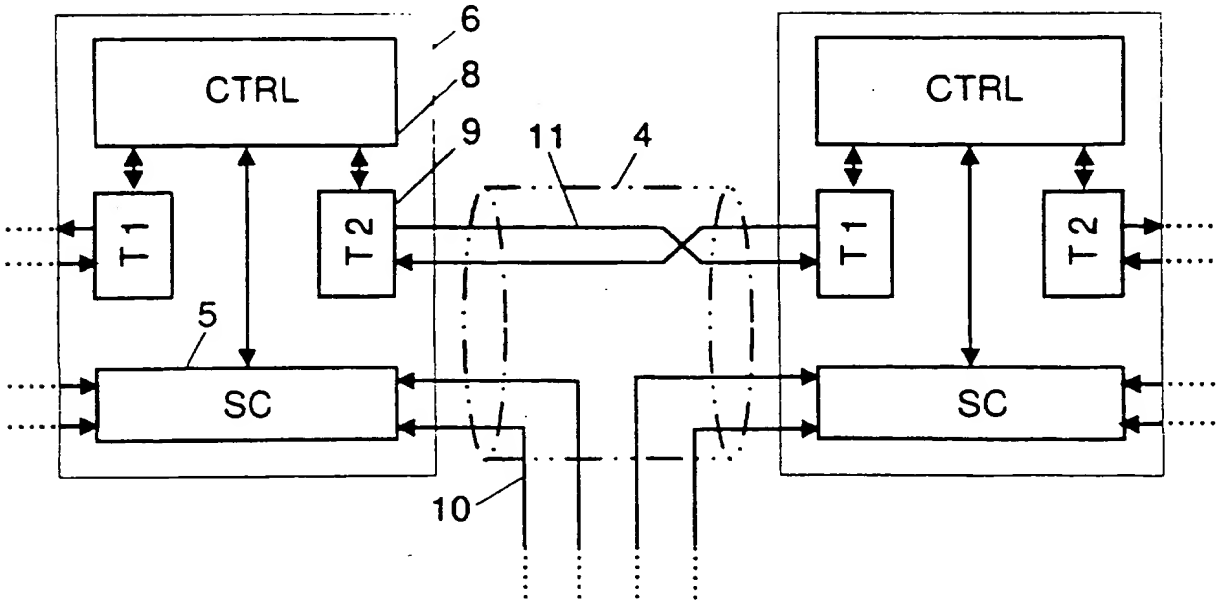
6
CTRL
8
9
11
4
CTRL
T1
T2
T1
T2
5
SC
SC
10

Fig.2

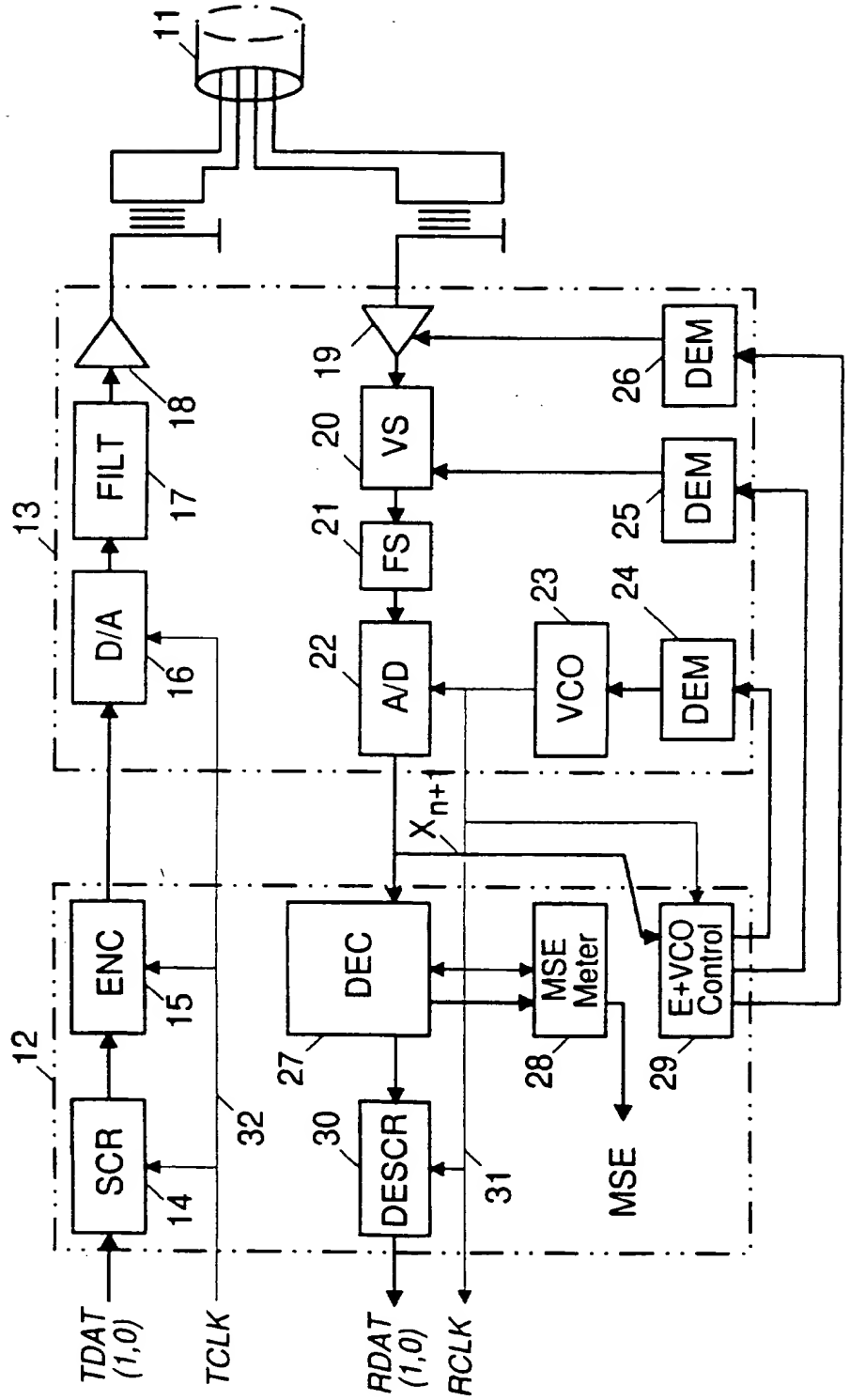
11
18
FILT
17
19
20
VS
21
FS
22
A/D
23
VCO
24
DEM
26
DEM
25
DEM
13
D/A
16
$X_{n+1}$
12
ENC
15
DEC
27
MSE Meter
28
E+VCO Control
29
SCR
14
32
30
DESCR
31
MSE
TDAT (1,0)
TCLK
RDAT (1,0)
RCLK

Fig.3

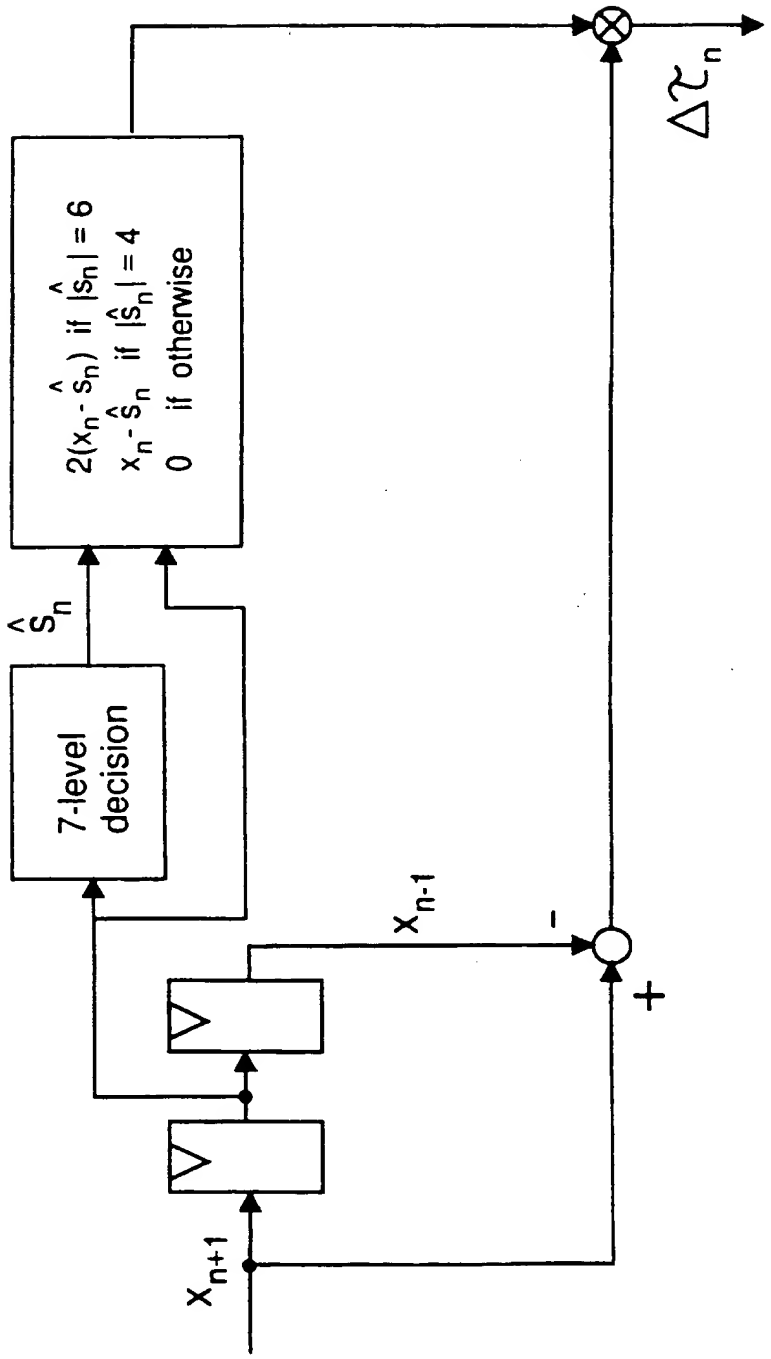
$\Delta\tau_n$
$2(x_n - \hat{s}_n)$ if $|\hat{s}_n| = 6$
$x_n - \hat{s}_n$ if $|\hat{s}_n| = 4$
0 if otherwise
$\hat{s}_n$
7-level decision
$x_{n-1}$
-
+
$x_{n+1}$

Fig.4

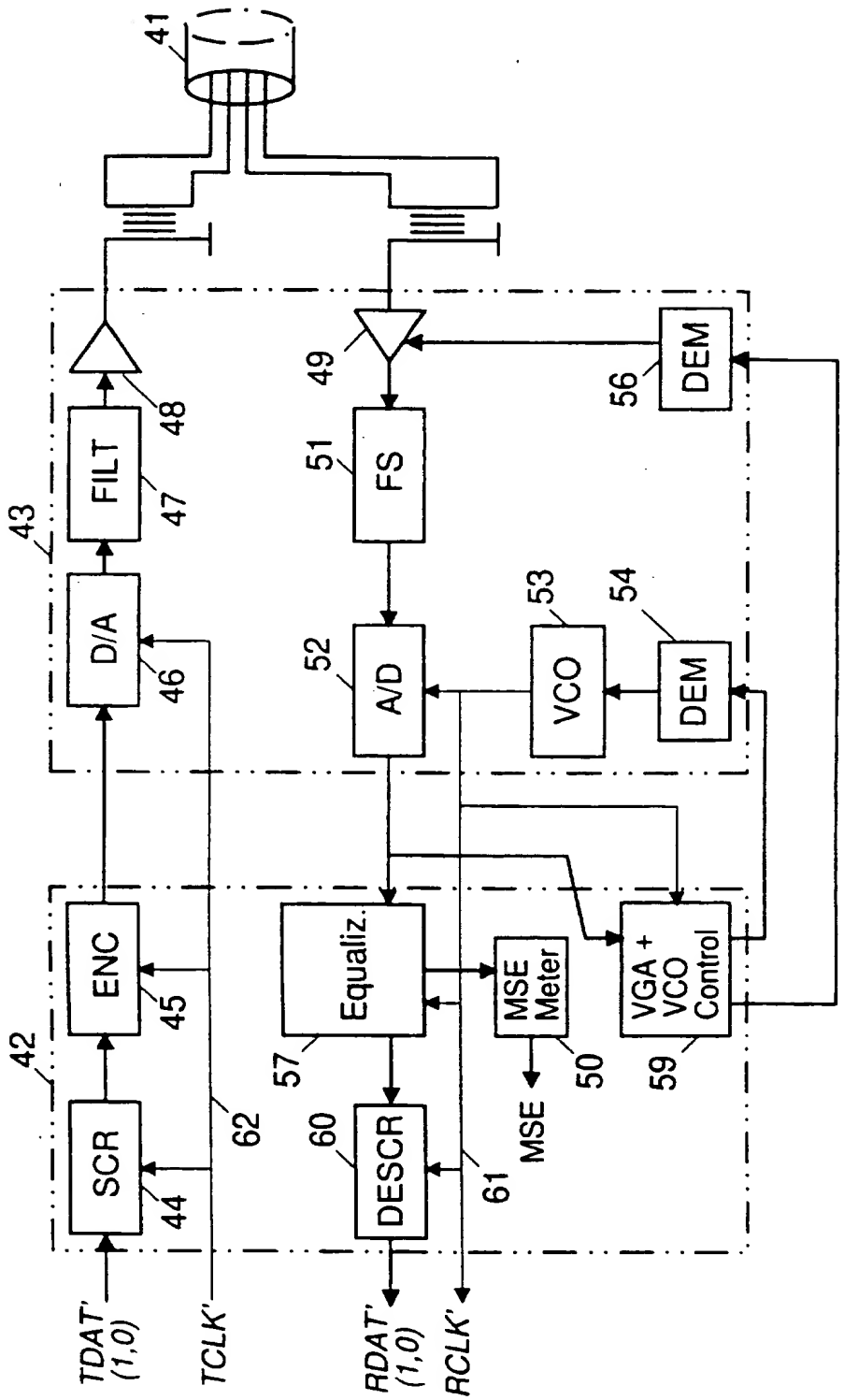


Fig.5

# INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/IB 96/00873

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L7/02 H04L25/497 H04L25/03

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | IEEE TRANSACTIONS ON COMMUNICATIONS, vol. 44, no. 6, 1 June 1996, pages 675-685, XP000599965 CHERUBINI G ET AL: "ADAPTIVE ANALOG EQUALIZATION AND RECEIVER FRONT-END CONTROL FOR MULTILEVEL PARTIAL-RESPONSE TRANSMISSION OVER METALLIC CABLES" see page 682, right-hand column - page 683, left-hand column, paragraph B see page 675, right-hand column, paragraph 3 - page 676, right-hand column, paragraph 1 see figure 1 --- | 1,2,4-6, 8,10,11 |
| A | EP 0 729 251 A (MATSUSHITA ELECTRIC IND CO LTD) 28 August 1996 see page 11, line 5 - line 28; figure 11 ----- | 1-3,8 |

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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| European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. ( + 31-70) 340-2040, Tx. 31 651 epo nl, Fax ( + 31-70) 340-3016 | Pieper, T |

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# INTERNATIONAL SEARCH REPORT

...ormation on patent family members

Intern al Application No
PCT/IB 96/00873

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| EP 0729251 A | 28-08-96 | JP 8237309 A | 13-09-96 |

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